FOUNDRY

Essential of Semiconductors

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WORKING EVERY DAY IN YOUR INTEREST AND FOR SOCIETY

INTRODUCTION

THE WORD “FOUNDRY” DEFINES COMPANIES THAT MANUFACTURE SEMICONDUCTORS OR CHIPS THROUGH A COMPLEX PROCESS

Foundries are part of the front-end semiconductor manufacturing. Some of the biggest fabs can produce over 100 000 wafers per month each containing multiple chips. These foundries play a key role in **the complex value chain**.

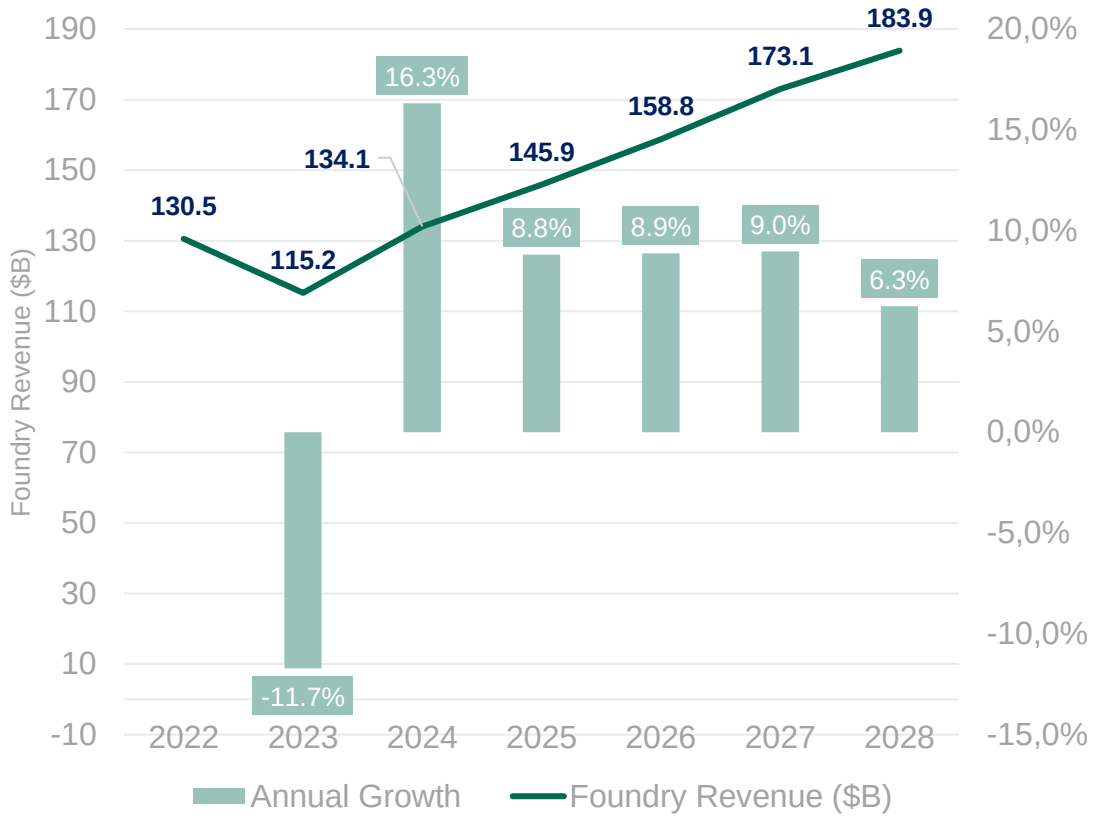
In 2023, foundries registered a $115.2 billion revenue with 92.5% of it being generated by the top 10 foundries of the market. TSMC, the industry leader, held a 60.1% revenue market share. The semiconductor industry recorded revenues of over $530 billion in 2023 and is expected to reach $823 billion by 2028.

Companies that use fabs as their main source of activity are called « **Pure-Play** » manufacturers (like TSMC). In contrast, companies that encompass other activities such as Design or ATP as well (Assembly, Test, and Packaging) are known as « **IDMs** » (Integrated Device Manufacturers). Historically, IDMs were **pioneers** of the semiconductor manufacturing industry but overtime as the industry fragmented new players dedicated to specific activities along the value chain emerged.

Foundries are high tech factories equipped with sophisticated equipment that perform automated steps. They follow **strict industry standards**. Each foundry is usually dedicated to **specific node sizes.** Therefore, it is crucial for foundries to consistently invest in new fabs to keep up with the semiconductor innovation race.

Between 2020 and 2023, **80 new semiconductor manufacturing projects** were announced solely in the United-States.

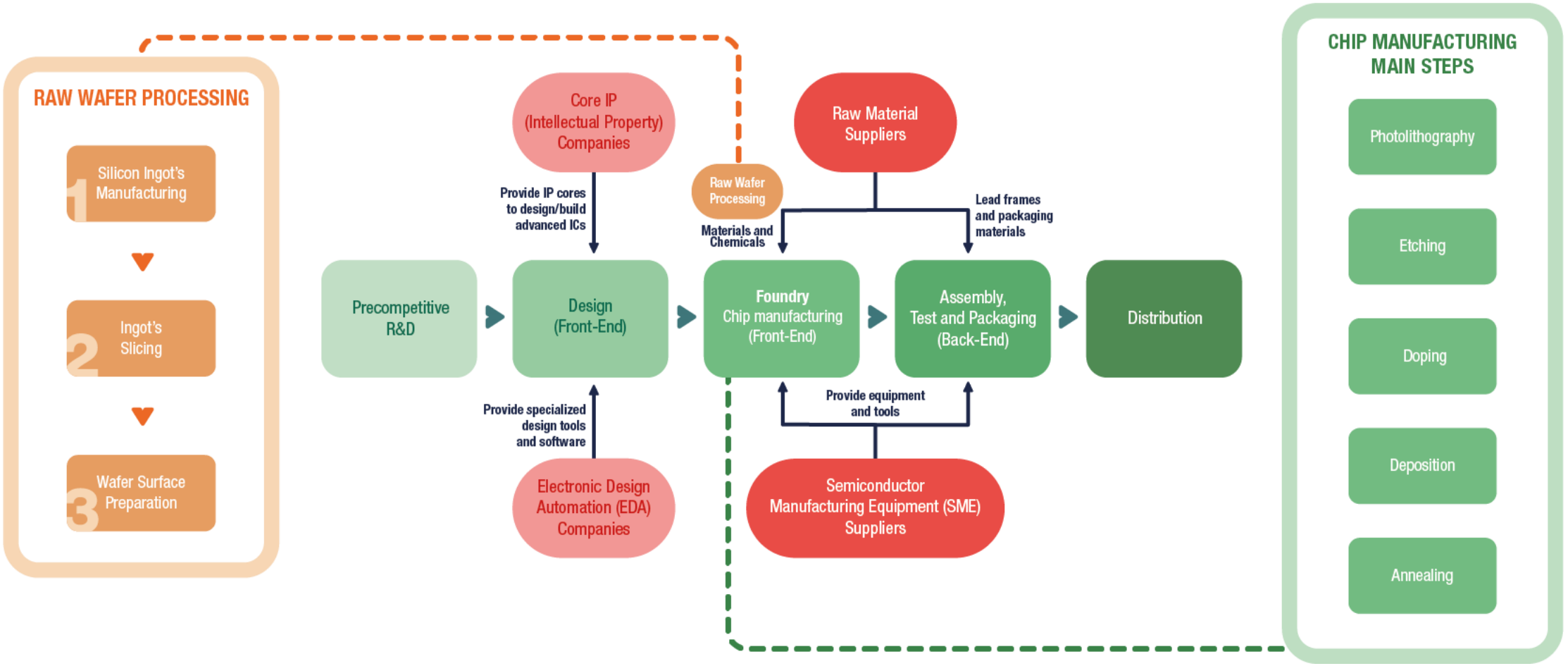
Figure 1 - Semiconductor Foundry Revenue ($B), Worldwide, 2022-2028



Sources: Gartner (July 2024), Crédit Agricole SA / ECO

SEMICONDUCTORS VALUE CHAIN

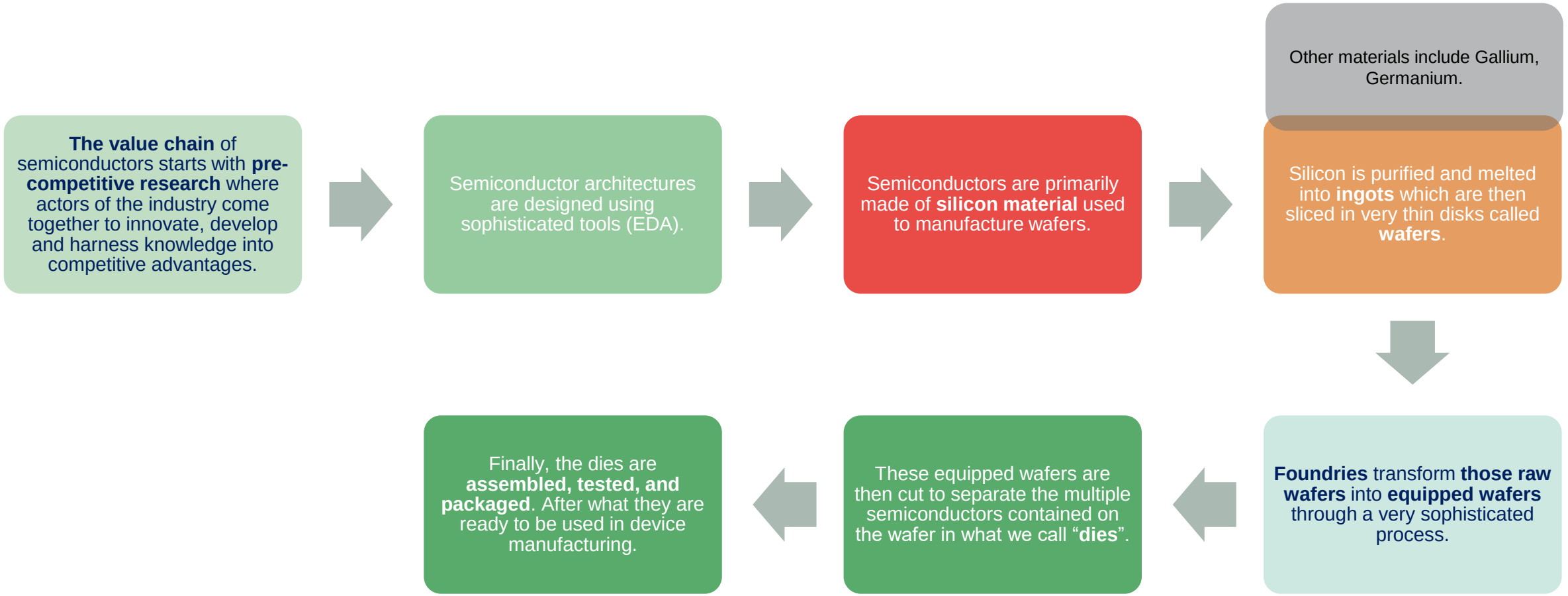
BASIC STRUCTURE: DESIGN / R&D, FOUNDRY, AND ATP



Sources: Global Value Chain Development Report 2023 (WTO), Crédit Agricole SA / ECO

SEMICONDUCTORS VALUE CHAIN

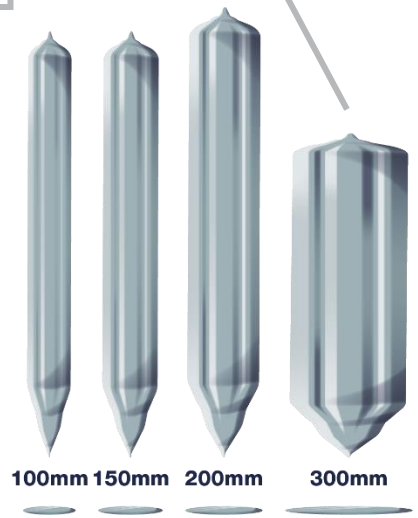
DESCRIPTION OF THE KEY BLOCKS OF THE BASIC VALUE CHAIN STRUCTURE



RAW WAFER PROCESSING

MANUFACTURING PROCESS OF RAW WAFERS

Standard wafer sizes: 150mm, 200mm, and 300mm – common size in use currently 300mm

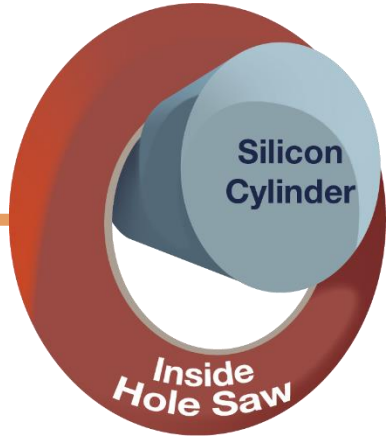


RAW WAFER PROCESSING

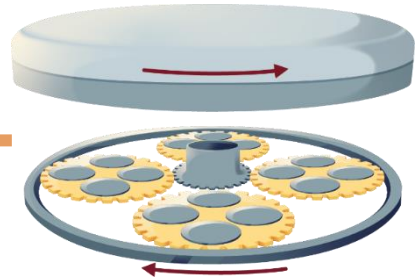
1. Silicon Ingot's Manufacturing
2. Ingot's Slicing
3. Wafer Surface Preparation

This initial step consists of extracting and purifying silicon to melt it and transform it into ingots using the **Czochralski Method.** The Czochralski Method is a highly precise technique essential for producing high-quality silicon wafers

Once the Ingots are made, in order for them to be shaped as wafers, they need to be sliced using specific techniques.

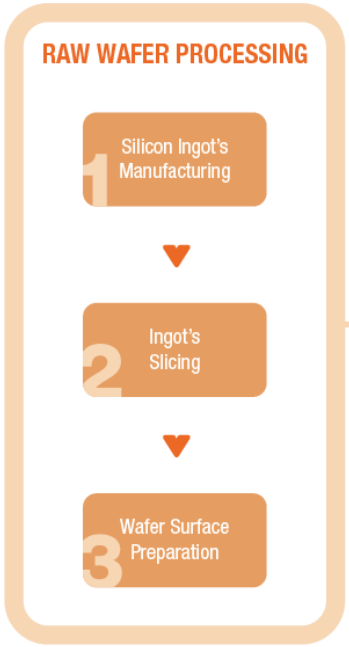


The final step of wafer processing consists of cleaning and testing the reliability of wafers before shipping them.

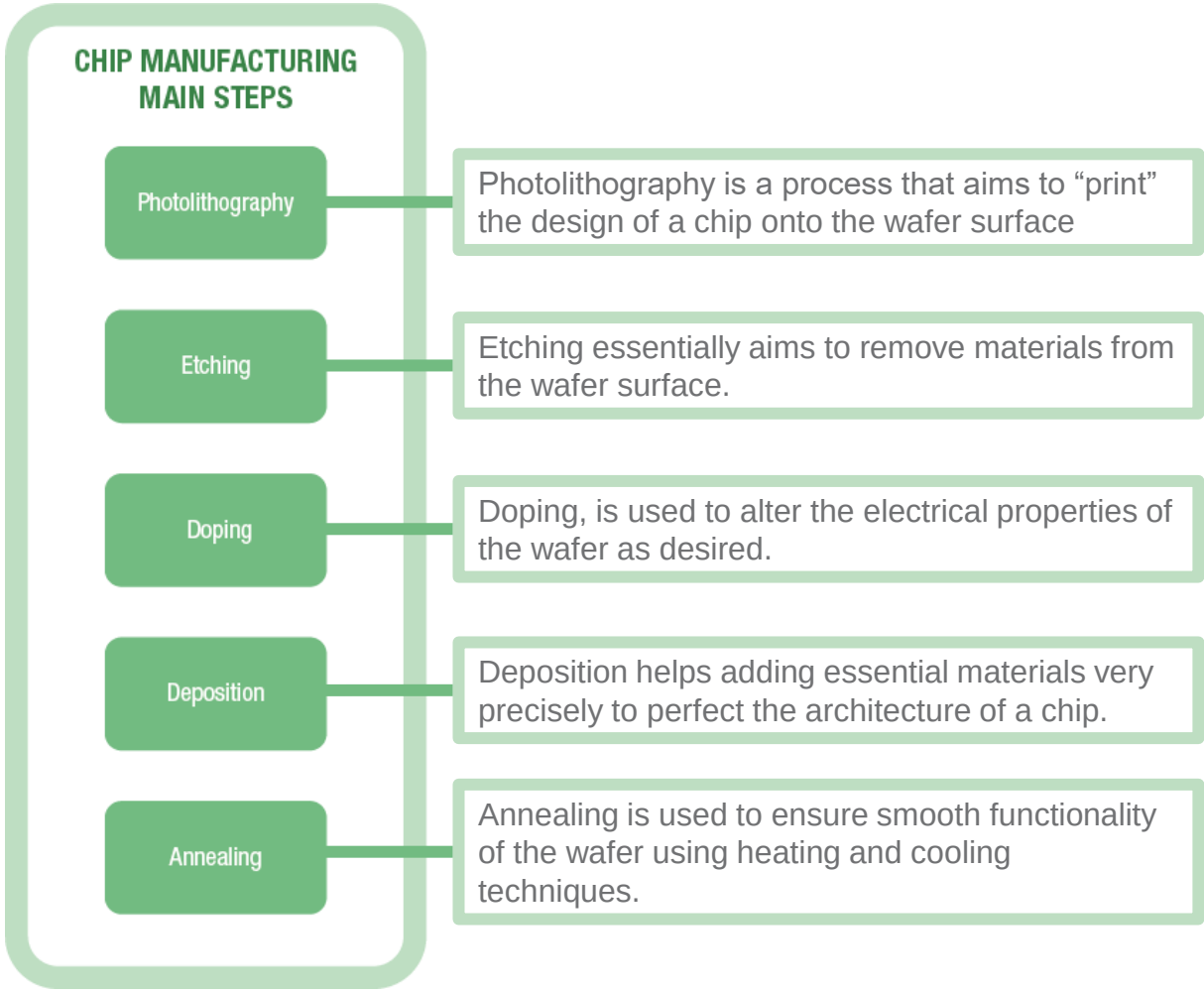


CHIP MANUFACTURING MAIN STEPS

DESCRIPTION OF MAIN MANUFACTURING STEPS (1/2)



- Once the wafers have been appropriately cleaned and successfully tested, **they are shipped to foundries** where they will be transformed into semiconductors.
- **There, they will go through several highly sophisticated processes multiple times** until they are ready to be assembled, tested, and distributed.
- **The process consists in the main following steps:** Photolithography, Deposition, Etching, Doping and Annealing.



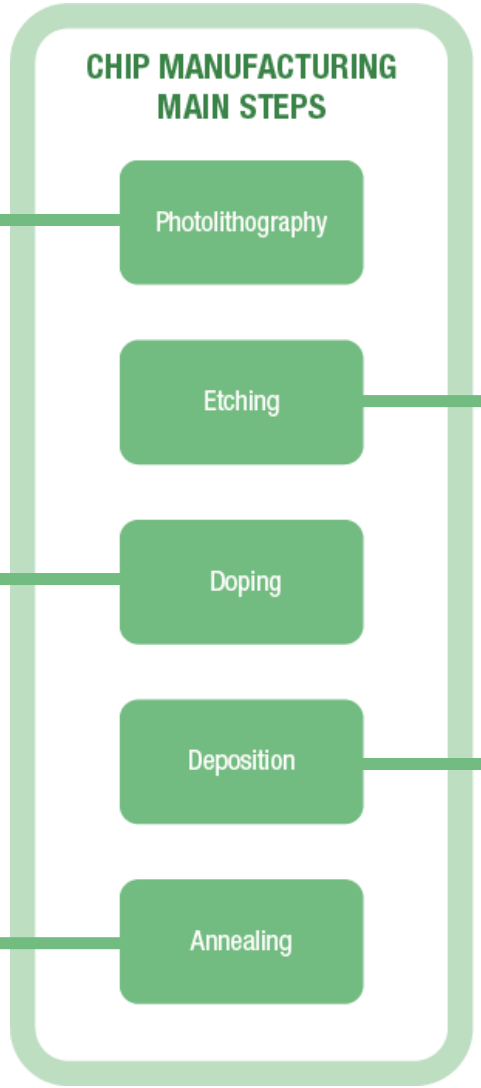
CHIP MANUFACTURING MAIN STEPS

DESCRIPTION OF MAIN MANUFACTURING STEPS (2/2)

The photolithography is arguably the central part of the semiconductor process. This method involves **projecting light onto the wafer surface through a reticle, known as a mask, and a lens to transfer the circuit patterns directly on the wafer (figure 2 – slide 12)**. Depending on the scale of the projected pattern, **deep or EUV lights** are used (figure 3 – slide 12) The precision requirements in photolithography are incredibly high, with submicron resolutions needed to create intricate circuit patterns.

Doping techniques are used to alter electrical properties of the semiconductor by introducing impurities onto the wafer surface. By adding specific impurities, the conductivity of the semiconductor can be modified, which is crucial for transistor formation. **One of the most common doping methods used is ion implementation**. In addition to doping, annealing is employed to ensure the quality of the dopants and repair any structural damage caused at the crystal level.

Annealing is a decisive step to ensure the optimization of material properties, general performances and quality control. During this process, the equipped wafer is subjected to controlled heating and cooling cycles.



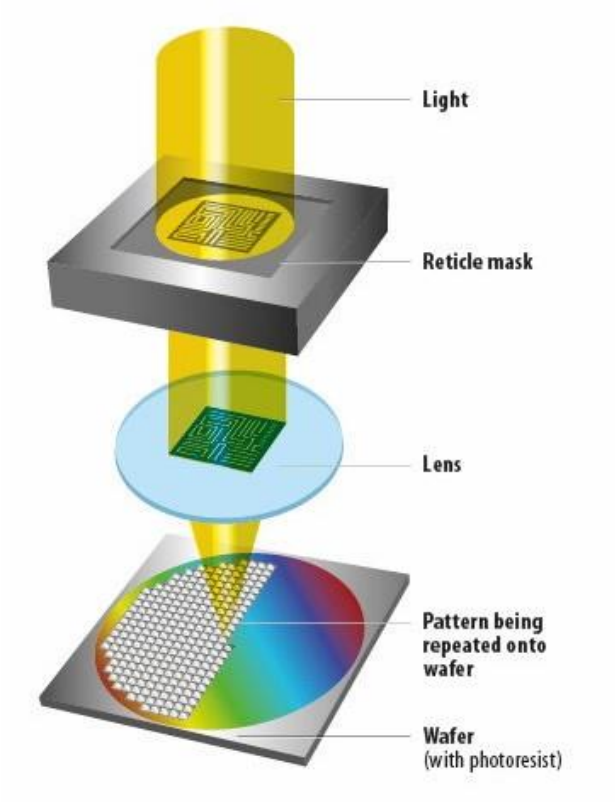
Etching processes help remove materials from the wafer surface, using resist materials and ion-based technologies to shape it according to the photomask pattern. The incredible precision of ion-based technologies is essential to ensure the integrity and functionality of the circuitry. Additionally, resist materials shield certain areas of the wafer surface from ion bombardment, serving as etching agents.

Deposition involves adding specific materials onto the wafer surface. To do so, two techniques are used. Chemical Vapor Deposition (**CVP**) and Physical Vapor Deposition (**PVD**). Like photolithography, deposition is crucial in the architecture of semiconductor chips. These techniques play an essential role in developing intricate patterns and structures for integrated circuits.

CHIP MANUFACTURING MAIN STEPS

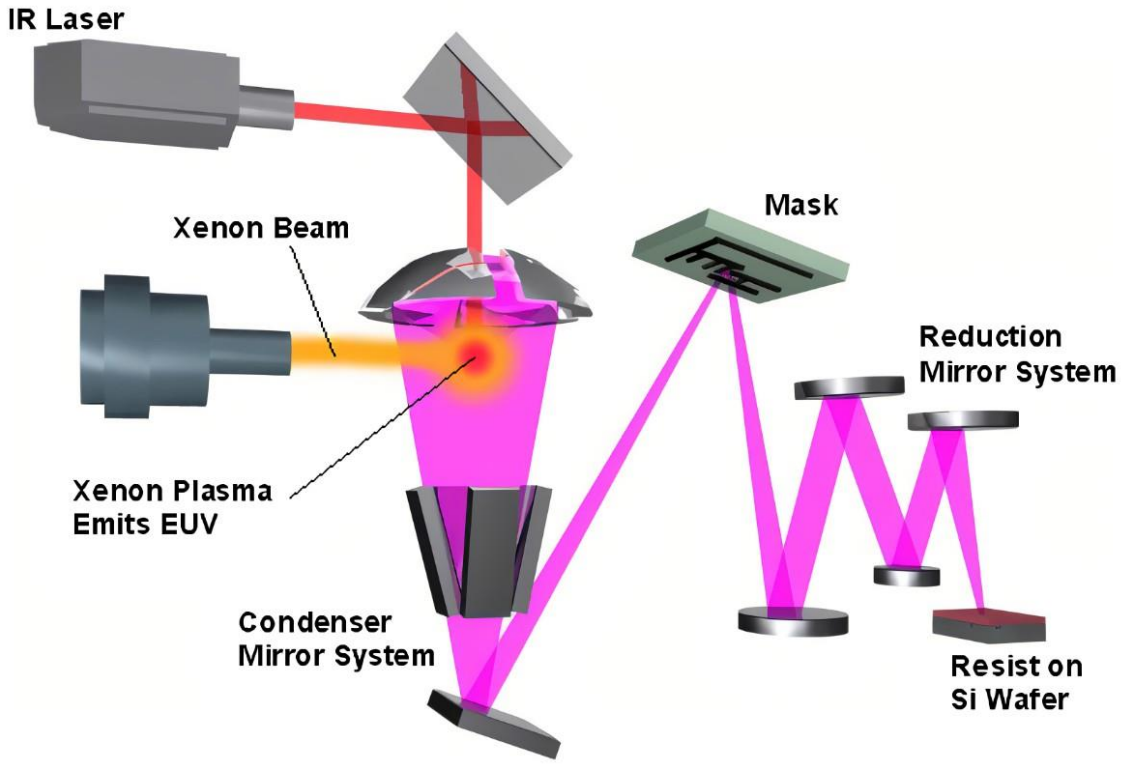
ILLUSTRATION OF PHOTOLITHOGRAPHY STEPS

Figure 2 – Simplified Photolithography Diagram



Sources : Control of lithography in semiconductor manufacturing (2006), Crédit Agricole SA / ECO

Figure 3 – Illustrative diagram of Extreme Ultra-Violet lights (EUV) lithography process



Sources : McGill University, Crédit Agricole SA / ECO

ASSEMBLY, TEST, AND PACKAGING (ATP)

ATP OR THE BACK-END PART OF THE VALUE CHAIN

Assembly, Test, and Packaging are the three steps that constitute the back-end manufacturing of semiconductors. These steps occur after the wafer transformation in dedicated facilities independent from foundries. The back-end manufacturing of a semiconductor represent the final stage of its production.

Once the wafers have gone through their transformation steps, chips (also known as ‘dies’) contained on wafers are almost ready to be separated. Before that, all transformed wafers need to undergo additional test called wafer sort. This step is designed to detect defective dies and identify compromised wafers.

Dies that function perfectly are then cut out individually from their original wafers (a process known as ‘**wafer dicing**’) and assembled into the specific system that they belong to. That process is called **assembly** and constitutes the first step of the back-end manufacturing process. Additionally, the dies need to be packaged carefully to ensure that no particles alter the properties and functionality of the chips. To ensure this, the dies are tested again. **Package testing involves functional tests, stress tests and performance verification.**

These batteries of tests are specific to packaged chips to ensure functionality until the end of the production prior to distribution.

Figure 4 - SPEA KGB Test Cells Automated Test Equipment

Sources: KGD Test Cells - Ensure KGD quality and performance | SPEA, Crédit Agricole SA / ECO

SEMICONDUCTOR MARKET – INTEL REGAINS ITS LEADING POSITION IN 2023

Due to an 11.7% decline, the global semiconductor market revenue was $530 billion in 2023. Recovery is expected to be **very strong** in 2024, with a growth of 19.2% driven by solid demand for **AI** and **Generative AI-related** applications by data centers. Furthermore, the market is expected to surpass the **$700 billion mark** by 2025. The semiconductor market is expected to grow at a CAGR of 9.2% from 2023 to 2028. Additionally, **semiconductor capacity** is projected to increase by over 60% from 2023 to 2030.

Intel is the **leading provider** of semiconductors worldwide, specializing in **compute electronics** and **data processing,** followed by Samsung 2nd and Qualcomm 3rd. Compute electronics remains the second-largest end-market for semiconductors and is expected to grow from $141 billion in 2023 to $244 billion in 2028. By doing so, it will surpass **communications electronics** which is currently the largest end market, standing at $159 billion in 2023 and forecasted to reach $226 billion in 2028.

Additionally, **memory systems**, which are designed to store data, are the most valuable type of semiconductor, representing 17% of semiconductor market revenue, amounting to nearly $92 billion in 2023. Memory systems are expected to reach $185 billion in 2028 with a CAGR of 15% between 2023 and 2028, accounting for 22% of market revenues.

Forecasts and prediction may be disturbed by three forces that could impact the semiconductor market: **Autonomy, Geopolitics** and **Electrical Power**. By 2030, ongoing constructions of high-performance compute projects for the development of AI-based applications could be limited by **power availability.**

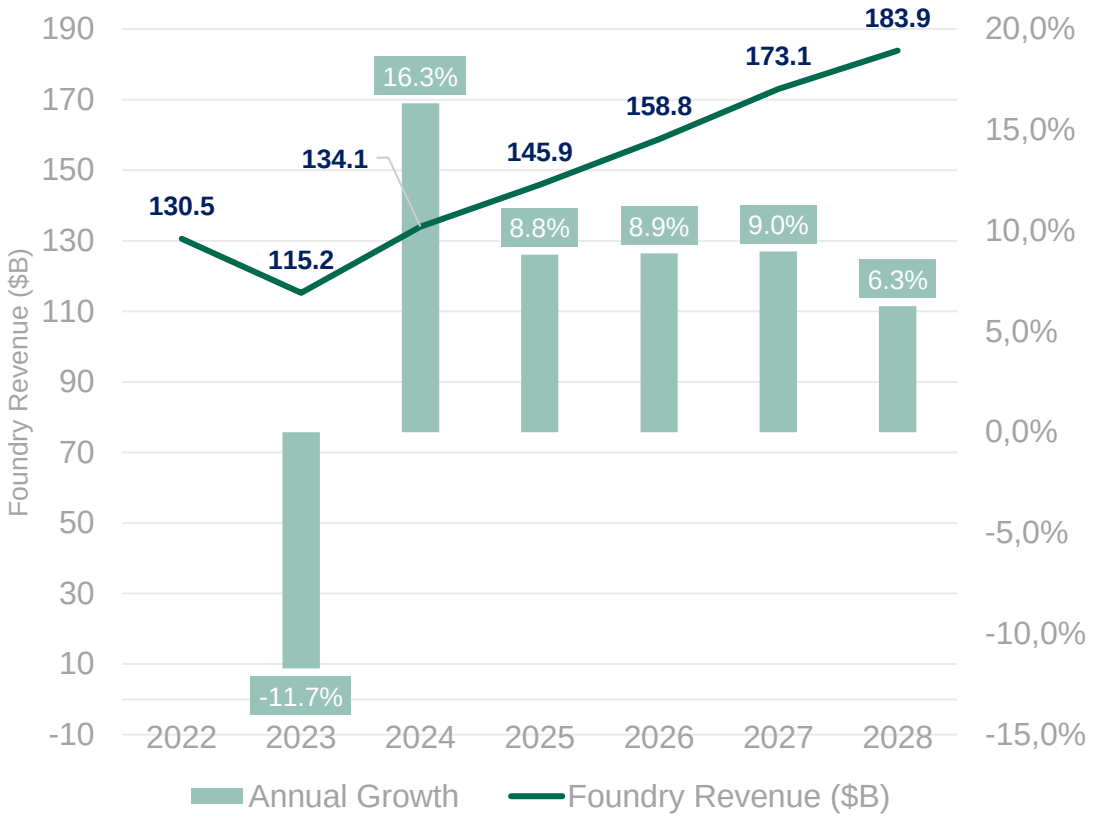
Figure 5 - Top Five Semiconductor Providers by Application, Worldwide
2023 Revenue (Millions of U.S. Dollars)

Sources: Gartner (April 2024), Crédit Agricole SA / ECO. Note: The value and size of the bubbles represent 2023 revenue ($ Millions).

MARKET OUTLOOK

FOUNDRY MARKET REACHED $115 BILLION IN 2023 AND IS EXPECTED TO STRONGLY REBOUND IN 2024

Figure 6 - Semiconductor Foundry Revenue ($B), Worldwide, 2022-2028



Sources: Gartner (July 2024), Crédit Agricole SA / ECO

Wafer fabrication, which constitutes the central part of semiconductor manufacturing, **exerts a pull effect on investments in other segment of the supply chain**. Its expensive capital and time requirements make it a priority for governments and industry leaders. **Forecast shows that between 2024 and 2032, around $2.3 trillion of private investment** will be dedicated to wafer fabrication, compared to $720 billion from 2013 to 2022.

In 2023, foundry revenues declined by 11.7% to $115.2 billion (opposite graph), following a 29.6% growth in 2022 ($130.5 billion). This decline can be explained by the decrease in low-end market demand due to reduced consumer electronics demand, resulting in fewer shipments of wafers getting out of foundries. However, despite this decline, **the foundry market revenue is expected to reach $184 billion in 2028, with a CAGR of 9.8% between 2023 and 2028.**

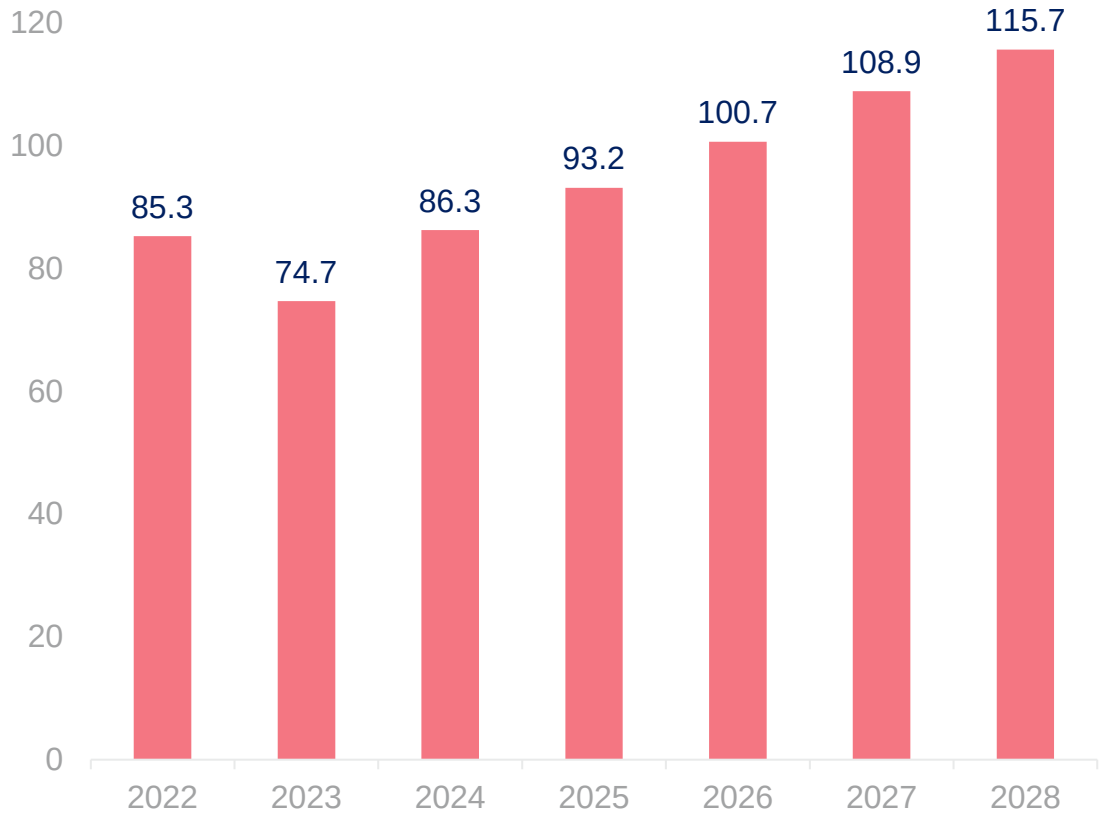
Furthermore, the average semiconductor capacity increase by region is projected to be 108% between 2022 and 2032, versus 81% from 2012 to 2022.

Overall, even though the trends in the foundry market in 2023 appear negative compared to 2022, **forecasts indicate a rebound in 2024 and steady growth thereafter until at least 2028.**

MARKET OUTLOOK

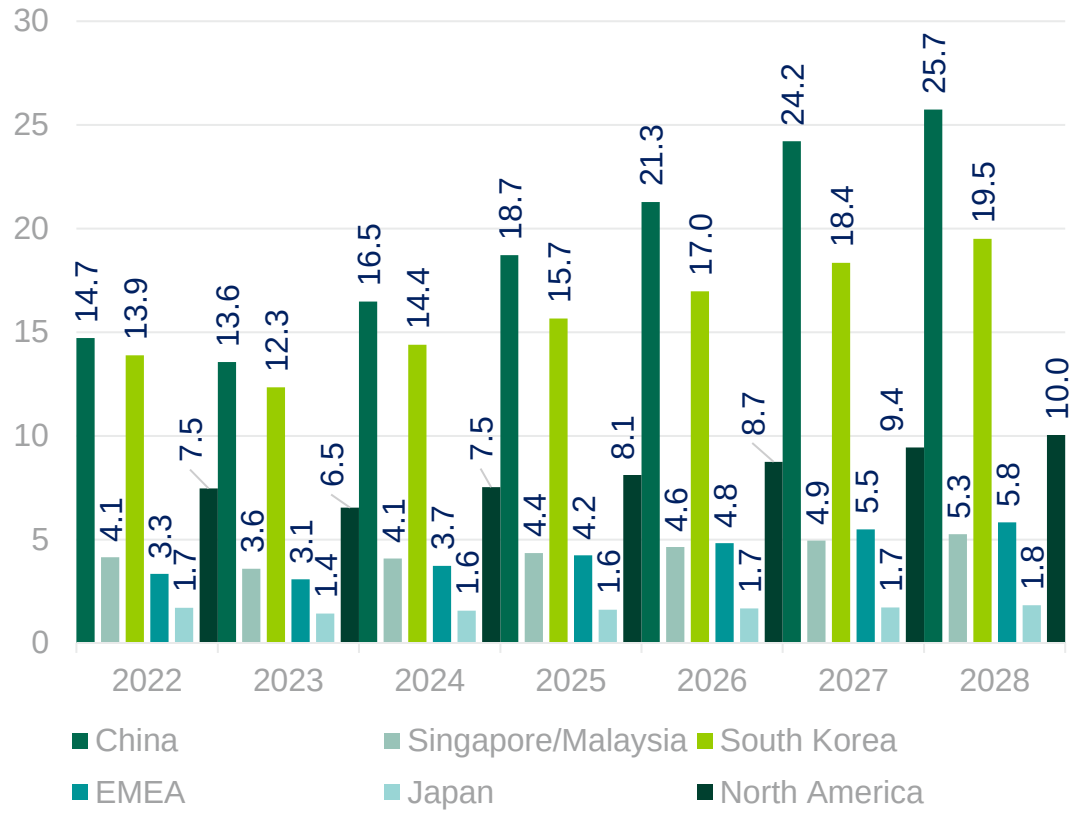
TAIWAN IS THE CLEAR LEADER OF THE FOUNDRY MARKET WITH ~$75 BILLION REVENUE IN 2023 AND 65% MARKET SHARE AND IS EXPECTED TO MAINTAIN ITS LEADERSHIP OVER THE PERIOD TO 2028

Figure 7 - Taiwan Foundry Revenue Forecast by Manufacturing Location, 2022-2028
Billions of dollar per year



Sources : Gartner (July 2024), Crédit Agricole SA / ECO

Figure 8 - Worldwide (Taiwan excluded) Foundry Revenue Forecast by Manufacturing Location 2022-2028
Billions of dollar per year



Sources : Gartner (July 2024), Crédit Agricole SA / ECO

MARKET OUTLOOK

TAIWAN LEADING WITH OVER 51% OF CURRENT WORLDWIDE FOUNDRY CAPACITY FOLLOWED BY CHINA WITH OVER 23%

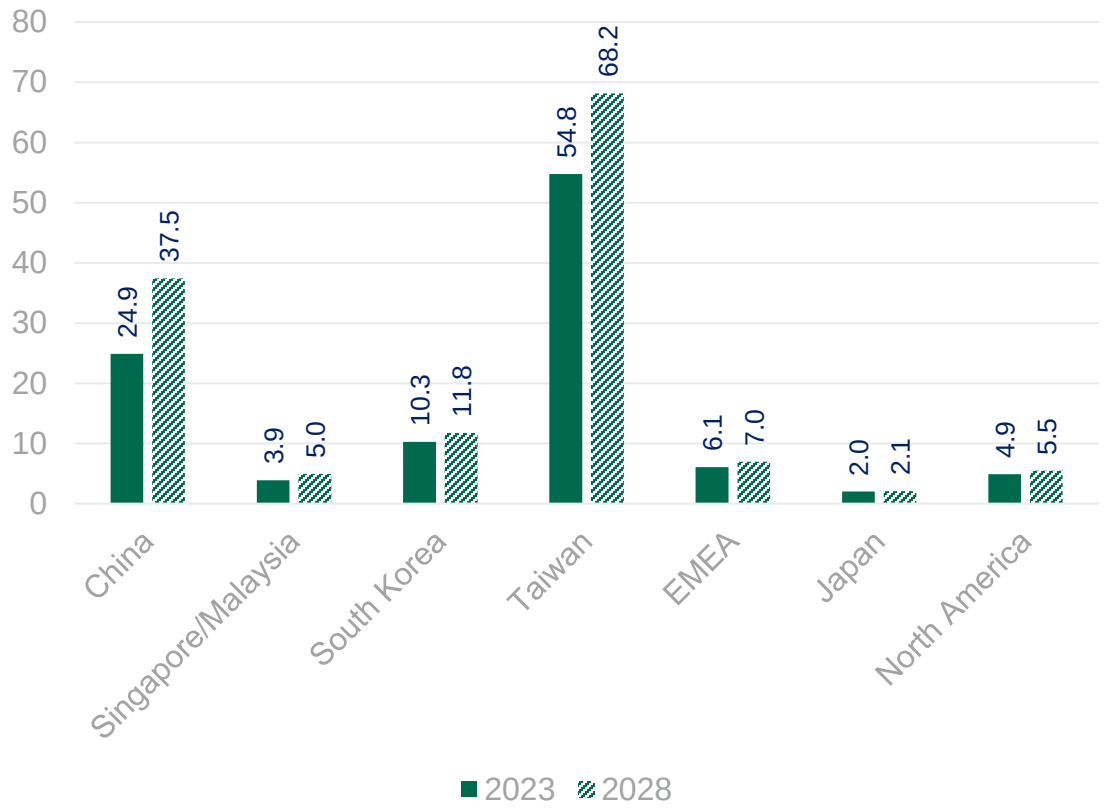
Taiwan is the industry leader with ~$75 billion in revenues in 2023 or ~65% market share and is anticipated to reach $116 billion in 2028 (CAGR 2023-2028 of 9.1%). China is second with ~$14 billion revenues in 2023 or ~12% market share, and is expected to reach ~$26 billion in 2028 (CAGR 2023-2028 of 13.7%). South Korea ranks third with over $12 billion revenues in 2023 or ~11% market share, and is anticipated to reach over $19 billion mark in 2028 (CAGR 2023-2028 of 9.6%).

China and EMEA are the two fastest growing geographies over the 2023-2028 period (CAGR of 13.7% for each). With $1.4 billion revenues in 2023, Japan has the smallest market share (1.2%).

Taiwan has the largest foundry capacity market share with 51.3% or 54.8 million 8-inch equivalent wafers manufactured in 2023. China follows with 25% market share or 24.9 million 8-inch equivalent wafers manufactured in 2023. South Korea is third with 9% market share or 10.3 million 8-inch equivalent wafers in 2023 (see opposite graph). **China will show fastest foundry capacity growth** with a CAGR 2023-2028 of 8.5%.

Regions like North America and Europe are benefiting from government incentives in order to build their own manufacturing capabilities and gain more strategic autonomy. The **American CHIPS Act** introduced in August 2022 is dedicating $52 billion in supporting the semiconductor industry. Since the bill passed in 2020, the United States attracted over $350 billion in private investment for semiconductor manufacturing according to BCG. Europe in turn, enacted in September 2023 the **E.U. CHIPS Act** which seeks to mobilize around €43 billion in public investments. The plan for Europe is to double their global manufacturing capacity from 10% to 20% by 2030.

Figure 9 - Worldwide foundry capacity forecast by region, 2023 / 2028
8-inch equivalent wafers (M) per year



Sources: Gartner (July 2024), Crédit Agricole SA / ECO

FOUNDRY – TOP 5 WITH 85.6% REVENUE MARKET SHARE, TSMC LEADING WITH 60.1% MARKET SHARE IN 2023

Figure 10 - Top Five Semiconductor foundry players by node size, Worldwide
2023 Revenue (Millions of U.S. Dollars)

Sources: Gartner (April 2024), Crédit Agricole SA / ECO. Note: The value and size of the bubbles represent 2023 revenue ($ Millions).

In 2023, **the top 10 accounted for 92.5% of revenue market share.**

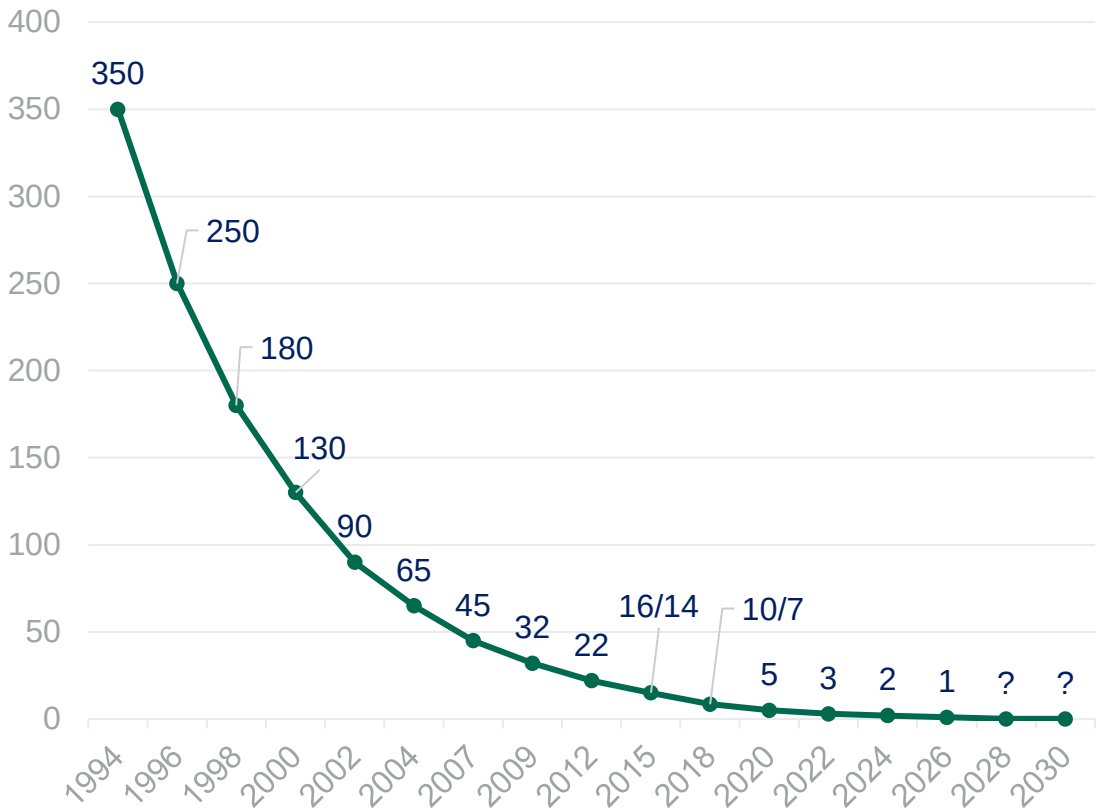
TSMC (Taiwan) maintained its position as the **undisputed leader** in foundry services with 60.1% of revenue market share in 2023, up from 58.1% in 2022, thereby gaining an additional 2% market share during a challenging year for the industry. TSMC continues to develop its expertise in the most advanced technologies **increasing its 3 nm capacity by 600%** (source: Gartner) and its 5 nm by 20% in 2023. Furthermore, TSMC is partnering with European clients in order to build foundry capacity in Europe for the benefit of both parties.

Samsung Electronics of South Korea (foundry services) ranks second with 7.4% market share closely followed by Global Foundries of the U.S. (6.4%). UMC (United Microelectronics Corporation) from Taiwan with 6,2% and SMIC (Semiconductor Manufacturing International Corporation) from China with 5.5% as illustrated in the opposite graph.

Most of foundry revenues are generated by shipments to **Americas** which is the favored location for TSMC accounting for 68% of its revenue ($47 billion in 2023). Of the top 5, four are Asian foundries and one is American, GlobalFoundries, which still has more than half of its facilities in Singapore. Therefore, the bulk of semiconductor manufacturing capabilities are **concentrated in Asia today.**

FOUNDRY – MOORE'S LAW IS REACHING ITS LIMITS AND INNOVATION LEADS TO NEW CHIP ARCHITECTURES

Figure 11 – Evolution of semiconductor node sizes throughout the years



Source:Stanford Nanoelectronics Lab, Wikichip, IEEE International Roadmap for Devices and Systems 2020, Crédit Agricole SA / ECO ; Note: Node sizes are in Nanometers (nm)

Foundries manufacture chips with different **technology nodes**, each requiring specific manufacturing processes. The smaller the technology node, the most advanced is the resulting semiconductor, featuring higher computing power, transistor density and power efficiency.

Historically, this statement was accurate as manufacturers named their technology nodes referring to the transistor **gate length**. However today, the meaning refers rather to a generation of chips using a specific technology.

The **Moore's law**, solely based on empirical observations by former CEO of Intel Gordon Moore back in 1965, suggests that the number of transistors in integrated circuits doubles every two years. After almost 60 years, this law is now reaching its limits. Some of the most **common technology nodes** available and used today are: 5nm, 7nm, 12nm, 14nm, 16nm, 65nm and others.

As a result, foundries need to adapt, and innovation is leading to new solutions as the industry moves forward. **Current transistors are largely based on FinFET (Fin Field Effect Transistor) architectures and are transitioning to nanosheet or GAA (Gate All Around) architectures**, expected to provide better device performance and lower power consumption, driving the next phase of semiconductor technology roadmap for 4nm/3nm chip manufacturing. **Further innovative solutions will be required as the industry moves to 2.5nm and 1.5 nm and below.**

Similarly, in the ATP segment of the value chain, Advanced Packaging technologies are gathering momentum. **While they may not be required systematically for all products, they can be a key product differentiator regarding features, performance, and cost.**

Nevertheless, different actors are specialized in different nodes with the leaders of the industry specializing in the more advanced ones (2nm, 3nm) like TSMC or Intel.

MARKET OUTLOOK

FOUNDRY – 3NM, 5NM, AND 7NM EXPECTED TO ACCOUNT FOR 43% OF REVENUE MARKET SHARE IN 2028

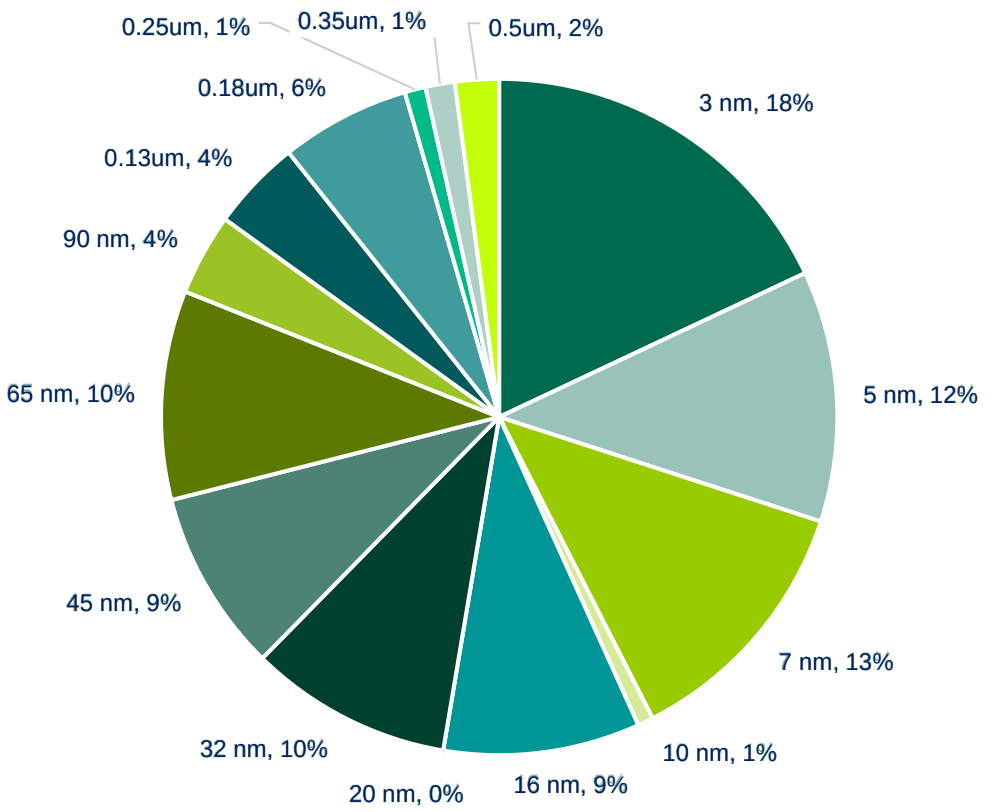
In 2023, the 5nm technology node generated the highest revenue for foundry services, amounting to approximately $23 billion. This single node accounted for 20% of all foundry revenues in 2024. Other significant revenue-generating nodes include the 7nm ($15 billion), 16nm ($11 billion), and 65nm ($12 billion) nodes. **High-end 2/3nm nodes are** expected to grow exponentially between 2023 and 2028 at a CAGR of 54.9%.

The rapid development of new nodes (5nm/3nm) leads to highest revenues from **3nm node in 2028 generating $33 billion or 18% revenue market share compared to $10 billion in 2024.** Additionally, the 5nm and 7nm nodes are expected to maintain substantial market shares, with 12% and 13% respectively, in 2028 (opposite graph).

Despite the 3nm, 5nm, and 7nm nodes holding the **largest cumulative market share with 43% in 2028**, their combined foundry capacity is anticipated to represent **only 12% of the total manufacturing capacity of all nodes**. In 2028, the 65nm node is projected to have the largest foundry capacity at 16%, followed by the 32nm node at 13% (figure 13 on next slide).

The most advanced technology nodes (3nm, 5nm, 7nm) generate the highest foundry revenues, though they are new leading-edge technologies only available with a few leading players.

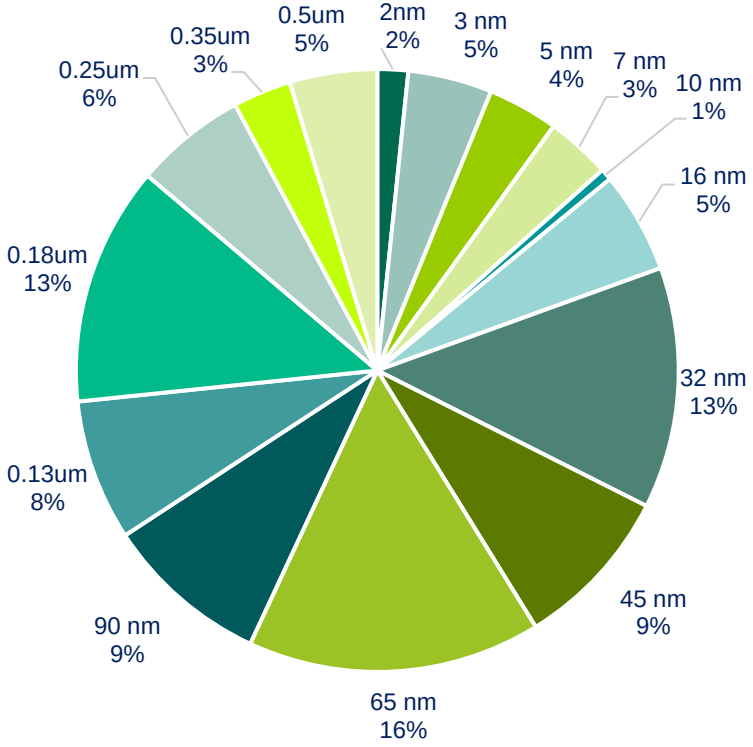
Figure 12 - Semiconductor Foundry Market Share Forecast (%) by Technology Node, 2028



Sources : Gartner (July 2024), Crédit Agricole SA / ECO

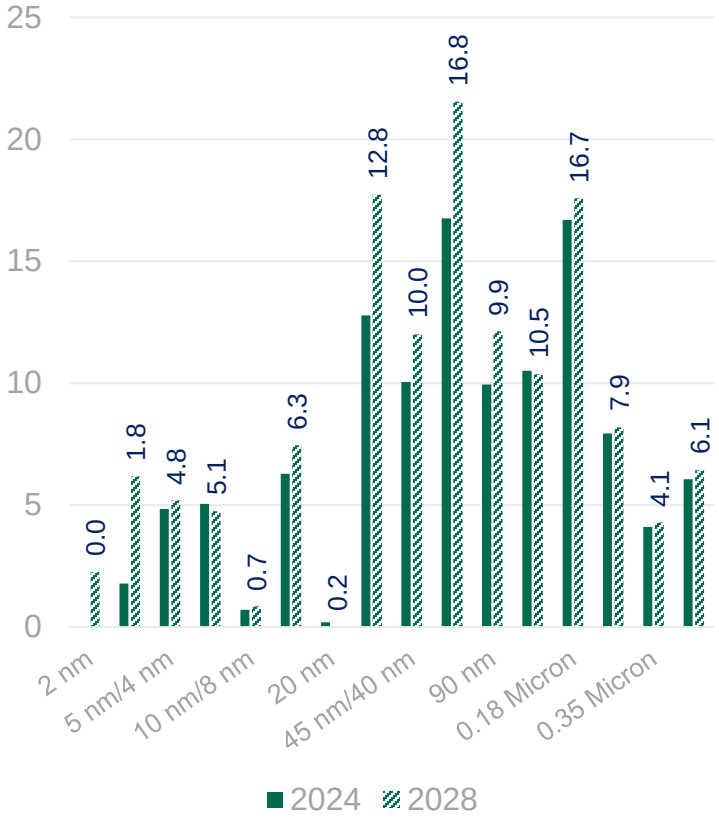
FOUNDRY – 3NM, 5NM, AND 7NM ACCOUNTING ONLY FOR 12% OF TOTAL FOUNDRY CAPACITY IN 2028

Figure 13 - Worldwide Foundry Capacity Forecast by Technology Node (%), 2028



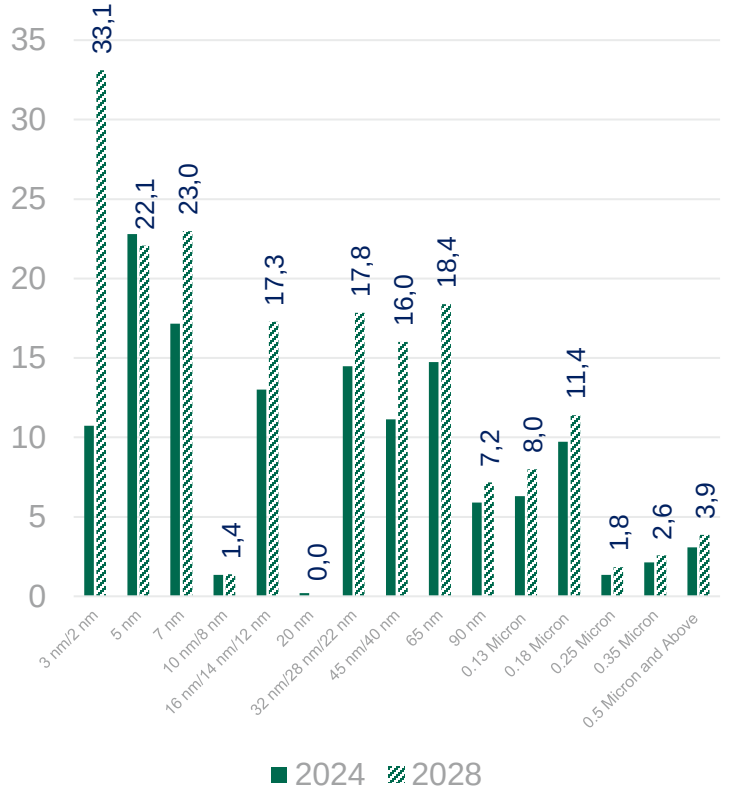
Sources: Gartner (July 2024), Crédit Agricole SA / ECO

Figure 14 - Worldwide Foundry Capacity Forecast by Technology Node (8-inch equivalent wafers (M) per year), 2024 / 2028



Sources: Gartner (July 2024), Crédit Agricole SA / ECO. Note: 1nm is 0.001 Micron

Figure 15 - Worldwide Foundry Revenue Forecast by Technology Node (*Billions of dollar per year*), 2024 / 2028



Sources: Gartner (July 2024), Crédit Agricole SA / ECO. Note: 1nm is 0.001 Micron

CHALLENGES

WORKFORCE SHORTAGES ARE INCREASING CHALLENGES IN FOUNDRY SERVICES AND MAY GET WORSE BY 2030

Workforce shortages are the most significant and concerning **challenges** for the semiconductor industry worldwide. With substantial incentives provided by governments and other entities, such as the **American or E.U. CHIPS act**, companies are eager to expand their capacity and build new production sites. Consequently, demand for workers is expected to grow considerably across the globe.

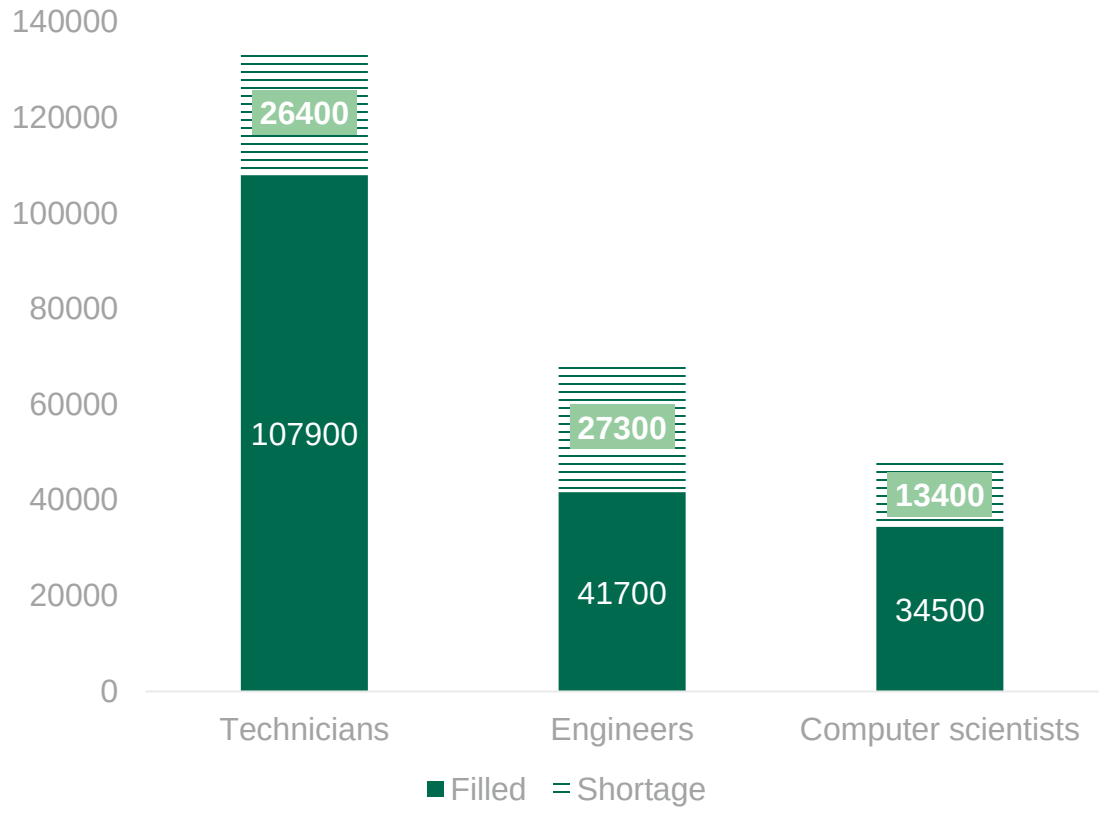
In fact, countries like South Korea are already experiencing these difficulties and are expecting them to get worse. The Ministry of Education reported a labor shortage of 1784 people in 2022, which is projected to reach 56 000 by 2031**. Over a period of nine years, the problem is anticipated to become 30 times worse,** a concerning figure for the Korean semiconductor industry.

In the U.S.A. the SIA (Semiconductor Industry Association) expects that by 2030, **58% of projected new jobs will go unfulfilled**. This means that 67 000 out of 115 000 jobs won't be operational, disrupting the U.S. semiconductor industry. TSMC, which recently started a new production plant in Arizona, has also encountered issues due to skilled workforce shortages. TSMC had no choice but to send over 500 technicians from Taiwan to the U.S. to train local labor adequately. As a result, the industry giant will have to wait **one more year for its $28 billion fab to be operational,** pushing the date to 2025 rather than 2024.

Intel for instance is tackling the issue head-on by partnering with state workforce groups and community colleges to train hundreds of technicians over the next five years. This initiative will start in Arizona and is expected to expand if successful.

Creating and developing training programs is an effective way of addressing the supply and demand workforce discrepancy. **Finding and retaining talent** is also crucial for these corporations that face significant challenges in the coming years.

Figure 16 - USA - Semiconductor occupational demand and gap summary, 2023–2030 total

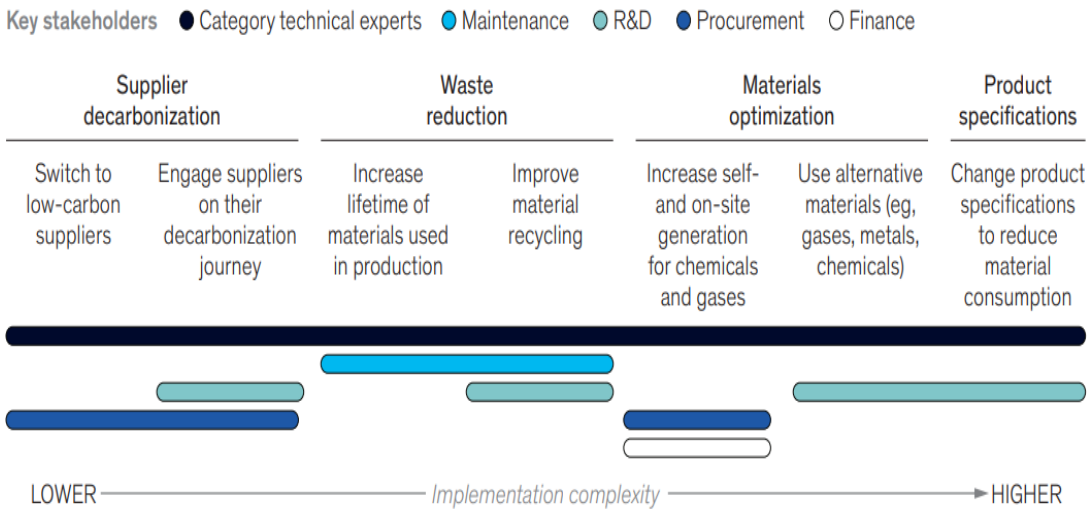


Sources: SIA (July 2023), Crédit Agricole ECO / SA

CHALLENGES

INNOVATION INDUSTRY FACES ENVIRONMENTAL CHALLENGES – SIGNIFICANT EFFORTS FROM TSMC AND UMC FOR RESOURCE USE AND EMISSIONS IMPROVEMENT BUT LACK OF ENVIRONMENTAL INNOVATION

Figure 17 – Scope 3 Decarbonization levers



Sources: McKinsey & Company, Crédit Agricole SA / ECO

65% of emissions from fabs fall into scope 1 (emissions directly created by companies) and scope 2 (emissions from the generation of purchased electricity, steam, heating, and cooling equipment). Within scope 1, processed gases account for **80%** of emissions, while in scope 2, facilities and tools fleets equally contribute to CO2 emissions for a typical fab. Foundries typically use gases such as PFCs, HFCs, NF3, and N20, which have high **Global-Warming Potential (GWP).**

Companies in the top 5 have each committed to reduce their carbon footprint and aim to comply with international laws and guidelines regarding global warming. Based on LSEG ESG Scoring Profile, TSMC, leader in the manufacturing industry, has a solid **ESG score of A- for FYE 2022,** with an average score of 84 over 5 years. Similarly, UMC (United Microelectronics Corp), ranked 4th in terms of revenue share, also holds an ESG score of A- as calculated by LSEG Eikon. However, the environmental pillar, which is critical to the ESG index, **is the lowest pillar for both companies, with a B+ rating (FYE 2022)** (see figure 18 on the following slide).

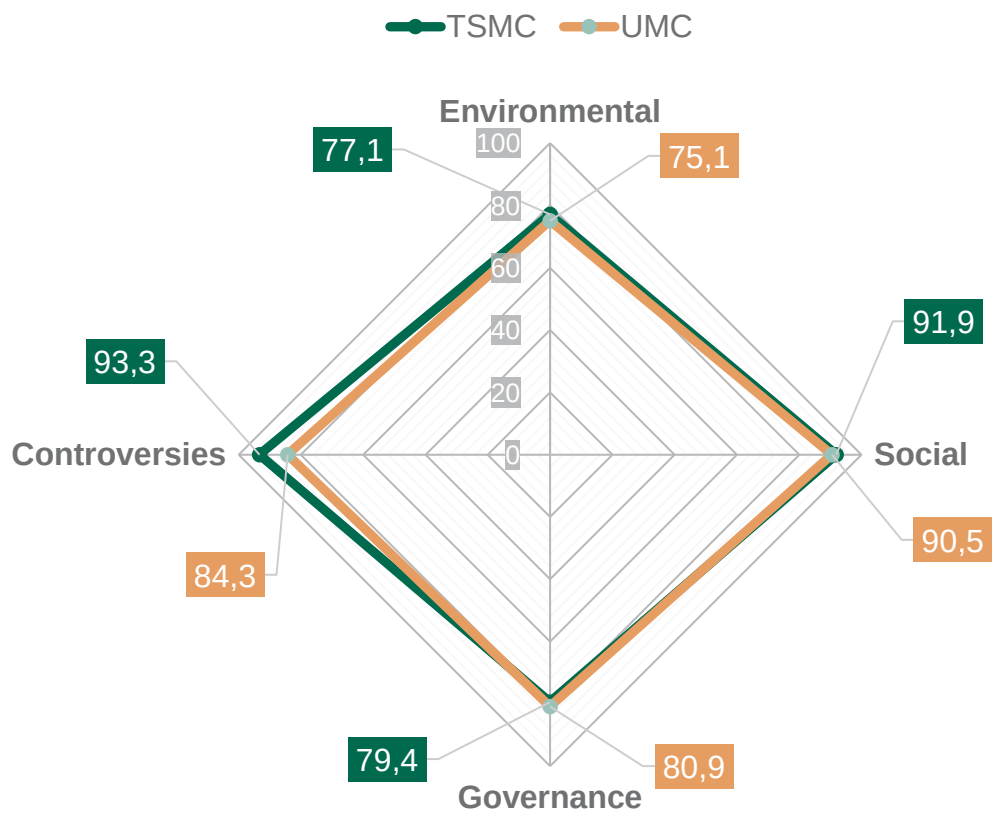
For both these companies, resource use and emissions, which together account for 19% of the ESG score, are **positive indicators of their commitment to reducing environmental impacts**. However, both companies score poorly in terms of **environmental innovations** (see Figure 19 on the following slide). This indicates that they do not perform efficiently in reducing environmental costs and burdens for their customers, nor do they excel in creating new market opportunities through environmental technologies, processes or eco-designed products.

According to McKinsey, scope 3 emissions, which include those generated by suppliers providing various services and materials to fabs, account for 35% of total emissions and may be one of the **most challenging issues to address**. In fact, these emissions are fragmented among hundreds of suppliers and materials, often beyond the reach of foundries. Therefore, foundries should aim to implement cooperative programs with suppliers, facilitate waste management and optimize the use of materials.

CHALLENGES

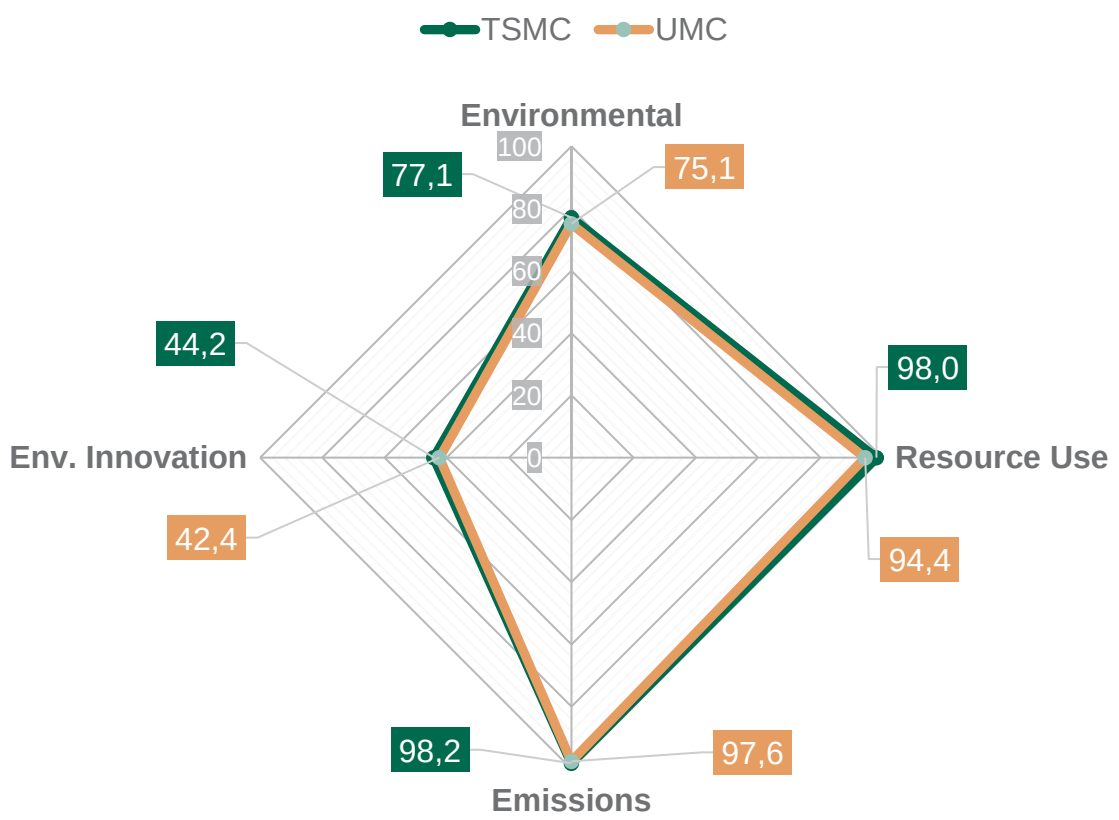
ENVIRONMENTAL – EXAMPLES OF RADAR MAPS FOR TSMC AND UMC

Figure 18 – LSEG 5-year average detailed ESG Score and ESG Controversies Score [2018-2022] TSMC and UMC



Sources: LSEG Eikon, Crédit Agricole SA / ECO

Figure 19 – LSEG 5-year average detailed ESG Environmental Pillar Score [2018-2022] TSMC and UMC



Sources: LSEG Eikon, Crédit Agricole SA / ECO

GLOSSARY

Fabs: Fabs are fabrication plants in which raw wafers are transformed into equipped wafers through several complex techniques.

TSMC: Taiwan Semiconductor Manufacturing Company

ATP: Assembly, Test, and Packaging

IDM: Integrated Device Manufacturer

IP: Intellectual Property

EDA: Electronic Design Automation

SME: Semiconductor Manufacturing Equipment

EUV: Extreme Ultra-Violet

CVP: Chemical Vapor Deposition

PVD: Physical Vapor Deposition

Si: Silicon

AI: Artificial Intelligence

CAGR: Compound Annual Growth Rate

UMC: United Microelectronics Corporation

SMIC: Semiconductor Manufacturing International Corporation

FinFET: Fin Field Effect Transistor

GAA: Gate All Around

SIA: Semiconductor Industry Association

PFCs: “PFCs” can be an abbreviation for either perfluorinated chemicals, or a subset of perfluorinated chemicals called perfluorocarbons.

HFCs: Hydrofluorocarbons (HFCs) are synthetic organic compounds that contain fluorine and hydrogen atoms.

NF3: the formula NF3 refers to Nitrogen trifluoride an inorganic compound.

N2O: This chemical formula refers to nitrous oxide

GWP: Global-Warming Potential

LSEG: London Stock Exchange Group

ESG: Environmental, Social and Governance

FYE: Fiscal Year End

E.U.: European Union

U.S.: United States

U.S.A.: United States of America

ECO
ÉTUDES ÉCONOMIQUES GROUPE

THANKS FOR YOUR ATTENTION

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